In the Claims:

Please cancel claim 1 without prejudice.

Please amend claims 2, 3, 6, 7, 9, 10, 11, 14, 18 and 19 as follows:

1. (canceled)

2. (currently amended)   A redundancy circuit for a memory array as recited in ~~claim 1~~ claim 3 includes a wordline select circuit coupled to said redundant driver for selecting a redundant wordline responsive to said enable redundant wordline signal.

3. (currently amended)   A redundancy circuit for a memory array ~~as recited in claim 1 wherein~~ comprising:

a miscompare detector for comparing a current address to be accessed with a memory defect address; said miscompare detector providing an enable redundant wordline signal responsive to a match of the compared addresses; said miscompare detector ~~includes~~ including a plurality of compare field effect transistors coupled between a common precharge node and a common discharge node;

a deactivate driver circuit coupled to said miscompare detector for disabling non-redundant wordlines responsive to said enable redundant wordline signal; and

a redundant driver coupled to said miscompare detector for enabling redundant wordlines responsive to said enable redundant wordline signal.

4. (original)   A redundancy circuit for a memory array as recited in claim 3 wherein said miscompare detector includes a precharge circuit coupled between a supply voltage and said common precharge node and a discharge device coupled between said common discharge node and ground.

5. (original) A redundancy circuit for a memory array as recited in claim 4 wherein one of said plurality of compare field effect transistors is activated, said common precharge node is discharged to identify a miscompare of the compared addresses and an access to a non-redundant wordline is allowed.

6. (currently amended) A redundancy circuit for a memory array as recited in ~~claim 1~~ claim 3 wherein said match of the compared addresses is identified by said plurality of compare transistors being deactivated, said common precharge node is maintained in a precharge state.

7. (currently amended) A redundancy circuit for a memory array as recited in ~~claim 1~~ claim 3 includes for each redundant wordline a miscompare detector for a wordline read address and a miscompare detector for a wordline write address.

8. (original) A redundancy circuit for a memory array as recited in claim 7 wherein said deactivate driver circuit receives a common precharge node signal for each said read address miscompare detector and each said write address miscompare detector.

9. (currently amended) A redundancy circuit for a memory array as recited in ~~claim 1~~ claim 3 wherein said deactivate driver circuit generates a reset signal to deactivate a non-redundant wordline decoder responsive to said enable redundant wordline signal.

10. (currently amended) A redundancy circuit for a memory array ~~as recited in claim 1 wherein~~ comprising:

a miscompare detector for comparing a current address to be accessed with a

memory defect address; said miscompare detector providing an enable redundant
wordline signal responsive to a match of the compared addresses;

a deactivate driver circuit coupled to said miscompare detector for disabling non-
redundant wordlines responsive to said enable redundant wordline signal; said
deactivate driver circuit ~~includes~~ including a two-high field effect transistor stack
coupled between a reset common node and ground; and

a redundant driver coupled to said miscompare detector for enabling redundant
wordlines responsive to said enable redundant wordline signal.

11. (currently amended)   A redundancy circuit for a memory array as recited in
claim 10 wherein said deactivate driver circuit couples said ~~enable redundant wordline~~
~~signal~~ common precharge node signal to said two-high field effect transistor stack to
discharge said reset common node responsive to said match and ~~generate~~ generates a
reset signal to deactivate a non-redundant wordline decoder.

12. (original)   A redundancy circuit for a memory array as recited in claim
10 wherein said deactivate driver circuit includes a keeper circuit coupled to said reset
common node.

13. (original)   A redundancy circuit for a memory array as recited in claim
10 wherein said deactivate driver circuit includes a saver transistor coupled to said reset
common node; said saver transistor being constantly activated and said saver transistor
providing said reset common node in a precharged state when said deactivate driver
circuit is activated.

14. (currently amended)   A redundancy circuit for a memory array as recited in ~~claim 1~~ claim 10 wherein said redundant driver coupled to said miscompare detector for enabling redundant wordlines responsive to said enable redundant wordline signal includes a buffer circuit receiving said enable redundant wordline signal and providing a buffered enable redundant wordline signal output.

15. (original)   A redundancy circuit for a memory array as recited in claim 2 wherein said wordline select circuit coupled to said redundant driver for selecting a redundant wordline responsive to said enable redundant wordline signal includes a wordline select circuit for a wordline read address and a wordline select circuit for a wordline write address; said wordline select circuit for said wordline read address and said wordline select circuit for said wordline write address coupled to said deactivate driver circuit.

16. (original)   A redundancy circuit for a memory array as recited in claim 15 wherein said wordline select circuit for said wordline write address includes a dynamic write node and said wordline select circuit for said wordline read address includes a dynamic read node; said dynamic write node and said dynamic read node being precharged responsive to a clock output signal generated by said deactivate driver circuit.

17. (original)   A redundancy circuit for a memory array as recited in claim 15 wherein said wordline select circuit for said wordline write address receives a write clock signal and said enable redundant wordline signal and said wordline select circuit

for said wordline read address receives a read clock signal and said enable redundant wordline signal.

18. (currently amended)   A method for disabling non-redundant wordlines and for enabling redundant wordlines using a redundancy circuit for a memory array comprising the steps of:

providing a miscompare detector having a plurality of compare field effect transistors coupled between a common precharge node and a common discharge node for comparing a current address to be accessed with a memory defect address;

said miscompare detector providing an enable redundant wordline signal responsive to a match of the compared addresses;

providing a deactivate driver circuit coupled to said miscompare detector, responsive to said enable redundant wordline signal, for generating a reset signal for disabling non-redundant wordlines; and

providing a redundant driver coupled to said miscompare detector, responsive to said enable redundant wordline signal, for activating a redundant wordline for said memory defect address.

19. (currently amended)   A method for disabling non-redundant wordlines and for enabling redundant wordlines as recited in ~~claim 19~~ claim 18 wherein said generated reset signal deactivates a wordline decoder for the memory array.

20. (original) A method for disabling non-redundant wordlines and for enabling redundant wordlines as recited in claim 19 includes the step responsive to a

miscompare of the compared addresses, of allowing a normal access to a non-redundant wordline.